ARRAY SUBSTRATE, TOUCH DISPLAY PANEL AND TOUCH DISPLAY DEVICE

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application claims priority to a Chinese patent application No. 201510600906.1 filed on Sep. 18, 2015 and entitled "Array Substrate, Touch Display Panel and Touch Display Device", the disclosure of which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] The present disclosure relates to the field of touch technologies, in particular to an array substrate, a touch display panel and a touch display device.

TECHNICAL BACKGROUND

[0003] Generally, a Thin Film Transistor Liquid Crystal Display (TFT-LCD) touch panel includes a display region and a non-display region located at the peripheral of the display region. FIG. **1** is a schematic view showing the structure of a non-display region of a TFT-LCD touch panel. Specifically, the non-display region **101** includes an Amorphous Silicon Gate (ASG) bus unit **103**, where the ASG bus unit **103** includes a plurality of signal buses for providing signals for gate lines, data lines and touch wires in the display region; and further includes an ASG capacitor unit **105** and an ASG thin film transistor unit **107** for receiving signals provide by the ASG buss. In normal, the ASG capacitor unit **105** has at least one capacitor, and two polar plates of the capacitor are generally made of light-proof metal materials, respectively, and hence it will significantly affect the light transmittance of the non-display region of the touch panel, thereby further affecting the curing effect of adhesive for sealing frames on the non-display region. In addition, the two polar plates of the capacitor in the ASG capacitor unit **105** are made of same materials to the material of gate lines and data lines in the display region, respectively, and are then made by the same etching process. Further, the plurality of signal buses in the ASG bus unit **103** in general are made of same material to that of the gate lines in the display region and then are made by the same etching process, or the plurality of signal buses in the ASG bus unit **103** are made of same material to that of the data lines in the display region and then are made by the same etching process. However, no matter which processing is selected, it is against to realize a narrow-frame design.

[0004] If the metal capacitor in the ASG capacitor unit **105** is manufactured as hollow-out shape, the light transmittance is increased, but the area of the wirings is wasted, and it is difficult to achieve a narrow-frame in that way. If the two polar plates of the capacitor in the ASG capacitor unit **105** are replaced with transparent metals, such as the tin indium oxide, this simple replacement may lead to a poor curing of the adhesives for sealing the frame, since the light transmittance of the tin indium oxide relative to the ultraviolet light is not relatively large even though the tin indium oxide has a relative large light transmittance. Furthermore, with the improvement of the resolution of the touch panel, the amount of the signal buses in the ASG bus unit **103** is increased, and the area occupied by the arrangement of the buses is larger. As a result, it is also difficult to achieve a narrow-frame in that way.

[0005] To sum up, for those skilled in the related art, there is a need for an array substrate in which the resolution is ensured while realizing the narrow-frame design.

SUMMARY OF THE INVENTION

[0006] In view of the drawbacks existing in the related art, the present disclosure provides a resolution as follows:

[0007] Embodiments of the present disclosure can provide an array substrate, including:

[0008] a substrate including a display region and a non-display region, where the display region includes a plurality of gate lines, a plurality of data lines and a plurality of touch leads; and a plurality of touch electrodes insulated from each other and electrically connected to the touch leads respectively. The non-display region can include: a first polar plate of a first capacitor and a second polar plate of the first capacitor, with the first capacitor being formed by overlapping the first polar plate of the first capacitor with the second polar plate of the first capacitor in a direction perpendicular to the substrate; and a first signal bus, which is partially overlapped with the first polar plate of the first capacitor and the second polar plate of the first capacitor in the direction perpendicular to the substrate.

[0009] The present disclosure also provides a touch display panel including the aforementioned array substrate.

[0010] The present disclosure also provides touch display device including the aforementioned touch display panel.

[0011] In the array substrate provided, the buses is configured as a structure which is partially overlapped with the capacitor in the non-display region in a direction perpendicular to the substrate, thereby further realizing the narrow-frame mode under the condition that the resolution is guaranteed.

DESCRIPTION OF DRAWINGS

[0012] In order to more clearly illustrate technical solutions in embodiments of the present disclosure, accompanying drawings used in the embodiments will be introduced briefly below. Obviously, accompanying drawings described below are merely some examples of the disclosure, and other accompanying drawings can be further obtained according to the accompanying drawings without any creative work for those ordinary skilled in the art,

[0013] FIG. **1** is a schematic view showing an exemplary structure of a non-display region of a TFT-LCD touch panel in the related art;

[0014] FIG. **2** is a top view of an array substrate according to an embodiment of the present disclosure;

[0015] FIG. **3**A is a top view of the wirings in a non-display region according to an embodiment of the present disclosure;

[0016] FIG. **3**B is a sectional view taken along a cut line AA' in FIG. **3**A;

[0017] FIG. **3**C is a sectional view taken along a cut line BB' in FIG. **3**A;

[0018] FIG. **3**D is a sectional view of the wirings in a non-display region according to an embodiment of the present disclosure;

[0019] FIG. **4**A is a sectional view of the wirings in a non-display region according to another embodiment of the present disclosure;

[0020] FIG. **4**B is a sectional view taken along a cut line CC' in FIG. **4**A;